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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,572	03/24/2004	Daniel C. Guterman	SNDK.138USM	7990

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PARSONS HSUE & DE RUNTZ LLP
655 MONTGOMERY STREET
SUITE 1800
SAN FRANCISCO, CA 94111

EXAMINER	
NGUYEN, VIET Q	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EF

Office Action Summary	Application No.	Applicant(s)	
	10/809,572	GUTERMAN ET AL.	
	Examiner	Art Unit	
	Viet Q. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Pre-Amendment filed on 3/24/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *42 and 43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42* is/are rejected.

7)☒ Claim(s) *43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/24/05 & 5/13/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **42-43** are present for examination.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim **42** is rejected under 35 U.S.C. 102(b) as being anticipated by **Park et al (5,768,188)**.

Park et al (see Fig.1) shows a non-volatile memory array structure which includes a plurality of non-volatile cells (T1-1 to T1-12). Col. 2 (see background) mentions that such memory cell could be used to store a multi-level data. For example, a cell can store two (N = 2) bits of information such that when N = 2 bits, there are four (4) possible information values (00, 01, 10, 11) can be stored by such cell for a total of 2^N distinct data storage levels (00, 01, 10, 11), and each such distinct level is capable of representative of a discrete 2-bit combination of logical data as well when **N >= 2** as claimed.

Regarding the claimed "stair-case" program-verify operation, Fig 6 (see col. 11-12) discusses the use of a stair-case program-verify pulses that are incremented and coupled to the memory cell gate for verifying the corrected threshold voltage level has been reached or not, and also to stop/inhibit such programming operation when such

cell reaches the predetermined storage level (00, 01, 10, or 11) as planned. For example, col. 11 (lines 56-67) stated that the program voltage is incremented by a 0.2 V interval and repeated with further verification until the threshold voltage is reached and a program inhibition is reached.

3. Claim **42** is rejected under 35 U.S.C. 102(b) as being anticipated by **Banks (5,218,569).**

Banks (see Fig.1) shows a non-volatile memory cell structure with a program,/floating gate. Col. 2 (see summary) mentions that such memory cell could be used to store a multi-level data. For example, a cell can store two (N = 2) bits of information such that when K = 2 bits, there are four (4) possible information values (00, 01, 10, 11) can be stored by such cell for a total of $\mathbf{2^N}$ distinct data storage levels (00, 01, 10, 11), and each such distinct level is capable of representative of a discrete 2-bit combination of logical data as well when **N >= 2** as claimed. Furthermore, this invention is applicable for all combinations of $\mathbf{K^n}$ where $\mathbf{K^n}$ is greater than two.

Regarding the claimed "stair-case" program-verify operation, Fig 11 (see col. 11-12) discusses the use of a stair-case program-verify pulses that are incremented and coupled to the memory cell program/gate, and for verifying the corrected threshold voltage level has been reached or not by using the comparison with a right reference voltage (Vref), and also to stop/inhibit such programming operation when such cell reaches the predetermined storage level (00, 01, 10, or 11) as planned. For example, col. 11 (lines 1-26) stated that the program voltage is incremented by fixed length timing

pulses, and the program voltage will be raised to respective levels, and such programming are also repeated with further verification until the threshold voltage is reached and a program inhibition is reached. The result is Fig.11 shows a stair-case programming/verification cycle as claimed.

4. Claim **43** contains allowable subject matter over prior arts of record because prior arts do not clearly teach or fairly suggest the use of a 'continuous" rang from a lowest Vt to a highest Vt that also includes an erased level and 2^N**-1** program levels, etc. as recited.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2827

V. Nguyen
5/29/2005